REMARKS

The following remarks are made in response to the Office Action mailed November 24, 2004. Claims 1-5 and 12-32 were rejected. Claims 6-11 have been objected to. With this Response, claims 2-5, 6-11, 18, 20, 23, 26, and 28-29 have been amended. Claims 19, 24, 25, and 27 have been cancelled. Claims 1-18, 20-23, 26, and 28-32 remain pending in the application and are presented for reconsideration and allowance.

Drawing Objections

The drawings are objected to because they do not show every feature of the invention specified in the claims. Figure 3 has been amended to remove the "COUNTER" text from block 112. Therefore, block 112 can represent either a counter or a shift register as disclosed in the Specification and Claims. Therefore, withdrawal of the objection to the drawings is respectfully requested.

Claim Rejections under 35 U.S.C. § 112

The Examiner rejected claims 5, 14, 20, and 29 under 35 U.S.C. § 112, second paragraph, as failing to set forth the subject matter which Applicant regards as their invention.

The drawings have been amended to show a shift register. Applicant respectfully submits that the above rejections under 35 U.S.C. § 112 should be withdrawn.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 1-5 and 12-32 under 35 U.S.C. § 102(e) as being anticipated by Borkenhagen et al. U.S. Patent No. 6,671,211.

Applicant submits that Borkenhagen fails to disclose the random access memory of claim 1. Claim 1 recites a random access memory. The random access memory comprises a latching circuit configured to receive a first signal and provide a second signal corresponding to the first signal to latch data signals into the random access memory, and a logic circuit configured to provide a first response after a predetermined number of the data signals have been latched into the random access memory by the second signal. The latching circuit is configured to receive

the first response and lock the second signal to a logic level based on the first signal and the first response to prevent inadvertent latching of other data signals.

Borkenhagen discloses a circuit for disabling a data latch from latching data whenever a data source is not driving the data strobe signal. (See Abstract). The circuit includes a DQS delay circuit 54 interposed between a DQS gate circuit 52 and a read data flow block 50. (Column 7, lines 44-48). To control gating of the DQS signal in DQS gate circuit 52, a pair of synchronous control signals DQS_ENABLE and DQS_POST are generated by a read sequencer in control logic 42. In addition, the source synchronous DQS signal is utilized in this gating function. Thus, a combination of synchronous and source synchronous signals are utilized to provide the gating functionality. (Column 7, lines 51-59). An AND gate 64 is utilized to gate the DQS signal using a DQS_GATE signal generated by a series of logic gates 66-70, resulting in the generation of a gated DQS signal applied to DQS delay block 54. Once delayed, the gated DQS signal is referred to as a delayed DQS signal, which is applied to one or more latches 56 in read data flow block 50. A latch is considered to be any circuitry that stores data signals from one or more DQ lines. (Column 8, lines 18-25).

Borkenhagen fails to disclose **a latching circuit configured to receive a first signal and provide a second signal corresponding to the first signal to latch data signals into the random access memory**, and **a logic circuit configured to provide a first response after a predetermined number of the data signals have been latched into the random access memory by the second signal, wherein the latching circuit is configured to receive the first response and lock the second signal to a logic level based on the first signal and the first response to prevent inadvertent latching of other data signals**. The Examiner submits that latching circuit 56 of Figure 4 in Borkenhagen discloses the latching circuit of claim 1. (Office Action, page 5). Latch 56, however, latches data from the DQs, it does not provide a second signal corresponding to the first signal to latch data signals into the random access memory. Latch 56 only receives the delayed DQS signal and does not provide any signals. Because the latching circuit 56 does not provide a second signal, the latching circuit cannot receive the first response from the logic circuit and lock the second signal to a logic level based on the first signal

and the first response. In view of the above, Applicant respectfully submits that the above rejection of claim 1 under 35 U.S.C. § 102(e) should be withdrawn.

Amended dependent claims depend directly or indirectly upon amended independent claim 9, indicated as having allowable subject matter. Accordingly, dependent claims 2-5 are also allowable over the art of record.

Applicant submits that Borkenhagen fails to disclose the random access memory of claim 12. Borkenhagen fails to disclose **a logic circuit configured to receive a clock signal and provide a first response after a predetermined number of clock edges have been received from the clock signal, a first latch configured to receive the first response in a first signal and provide a second response based on the first response and the first signal**, and **a second latch configured to receive the second response and the first signal and provide a corresponding second signal, wherein the second latch circuit is configured to lock the second signal to a logic level based on the second response and the first signal**. The Examiner submits that Figure 4 of Borkenhagen discloses a logic circuit configured to receive a clock signal and provide a first response after a predetermined number of clock edges have been received from the clock signal. (Office Action, page 6). The gating circuit 52, however, does not receive any clock signal. Gating circuit 52 receives a DQS signal, a DQS_ENABLE signal, and a DQS_POST signal, none of which are clock signals. The Examiner submits that the first latch circuit is disclosed by DQS gate circuit 52. (Office Action, page 6). The Examiner submits that the second latch is disclosed by latch 56. (Office Action, page 6). For the same reasons as discussed above with reference to claim 1, latch 56 does not disclose a second latch configured to receive the second response and the first signal and provide a corresponding second signal, because latch 56 does not provide any signals. In view of the above, Applicant respectfully submits that the above rejection of claim 12 under 35 U.S.C. § 102(e) should be withdrawn.

Dependent claims 13 and 15-17 depend directly or indirectly upon independent claim 12. Accordingly, dependent claims 13 and 15-17 are also allowable over the art of record.

Applicant submits that Borkenhagen fails to disclose the random access memory of amended independent claim 18. Borkenhagen fails to disclose **a locking circuit comprising a counter configured to be reset in response to a write command signal and count bursts of**

input data up to a burst length to determine that the input data is latched. This limitation includes the limitation of claim 7, which the Examiner has allowed if rewritten in independent form. In view of the above, Applicant respectfully submits that the above rejection of claim 18 under 35 U.S.C. § 102(e) should be withdrawn.

Applicant submits that Borkenhagen fails to disclose the random access memory of amended independent claim 20. Borkenhagen fails to disclose **a locking circuit comprising a shift register configured to start shifting in response to a write command signal and shift up to a burst length to determine that the input data is latched.** In view of the above, Applicant respectfully submits that the above rejection of claim 20 under 35 U.S.C. § 102(e) should be withdrawn.

Dependent claims 21 and 22 depend directly upon amended independent claim 18. Accordingly, dependent claims 21 and 22 are also allowable over the art of record.

Applicant submits that Borkenhagen fails to disclose the random access memory of amended independent claim 23. For the same reasons as discussed above with respect to claim 1, Borkenhagen fails to disclose the means for preventing comprising **means for indicating the first signals are latched, wherein the means for indicating provides an indication, and means for locking the second data strobe to a logic level based on the indication.** Borkenhagen also fails to disclose the means for locking comprises **means for latching a first output based on the first data strobe and the indication, and means for latching a second output based on the first data strobe and the first output, wherein the means for latching a second output locks the second data strobe to the logic level.** In view of the above, Applicant respectfully submits that the above rejection under 35 U.S.C. § 102(e) of claim 23 should be withdrawn.

Applicant submits that Borkenhagen fails to disclose the method of amended independent claim 26. Borkenhagen fails to disclose **indicating that a burst of data signals are received comprises counting positive edges of a clock signal after a write command up to a set value.** This limitation is similar to the limitation of claim 6, which the Examiner has allowed if rewritten in independent form. In view of the above, Applicant respectfully submits that the above rejection of claim 26 under 35 U.S.C. § 102(e) should be withdrawn.

Dependent claims 28, 31, and 32 depend directly upon independent claim 26. Accordingly, dependent claims 28, 31, and 32 are also allowable over the art of record.

Applicant submits that Borkenhagen fails to disclose the method of amended independent claim 29. Borkenhagen fails to disclose **indicating that a burst length of data signals are received comprises shifting a shift register for each data signal in the burst of data signals up to a set value**. In view of the above, Applicant respectfully submits that the above rejection of claim 29 under 35 U.S.C. § 102(e) should be withdrawn.

Dependent claim 30 further defines independent claim 29. Accordingly, dependent claim 30 is also allowable over the art of record.

Allowable Subject Matter

The Examiner objected to claims 6-11 for being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims. Claims 6-11 have been rewritten in independent form including the limitations of the rejected base claim 1. Accordingly, claims 6-11 are now in form for allowance. Applicant respectfully requests that the objections to claims 6-11 be withdrawn.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-18, 20-23, 26, and 28-32 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and objections and allowance of claims 1-18, 20-23, 26, and 28-32 is respectfully requested.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Respectfully submitted,

Jonghee Han,

By his attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-2002
Facsimile: (612) 573-2005

Date: February 24, 2005
SED:jan

Steven E. Dicke
Reg. No. 38,431

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 24 day of February, 2005.

By Steven E. Dicke
Name: Steven E. Dicke

IN THE DRAWINGS

Figure 3 has been amended as indicated in red in the attached annotated drawing sheet. In addition, a replacement sheet incorporating the amendment to Figure 3 is also attached.

ANNOTATED SHEET SHOWING CHANGES

Docket No.: 2003 P 52607 US

RANDOM ACCESS MEMORY WITH DATA STROBE LOCKING CIRCUIT

Jonghee Han

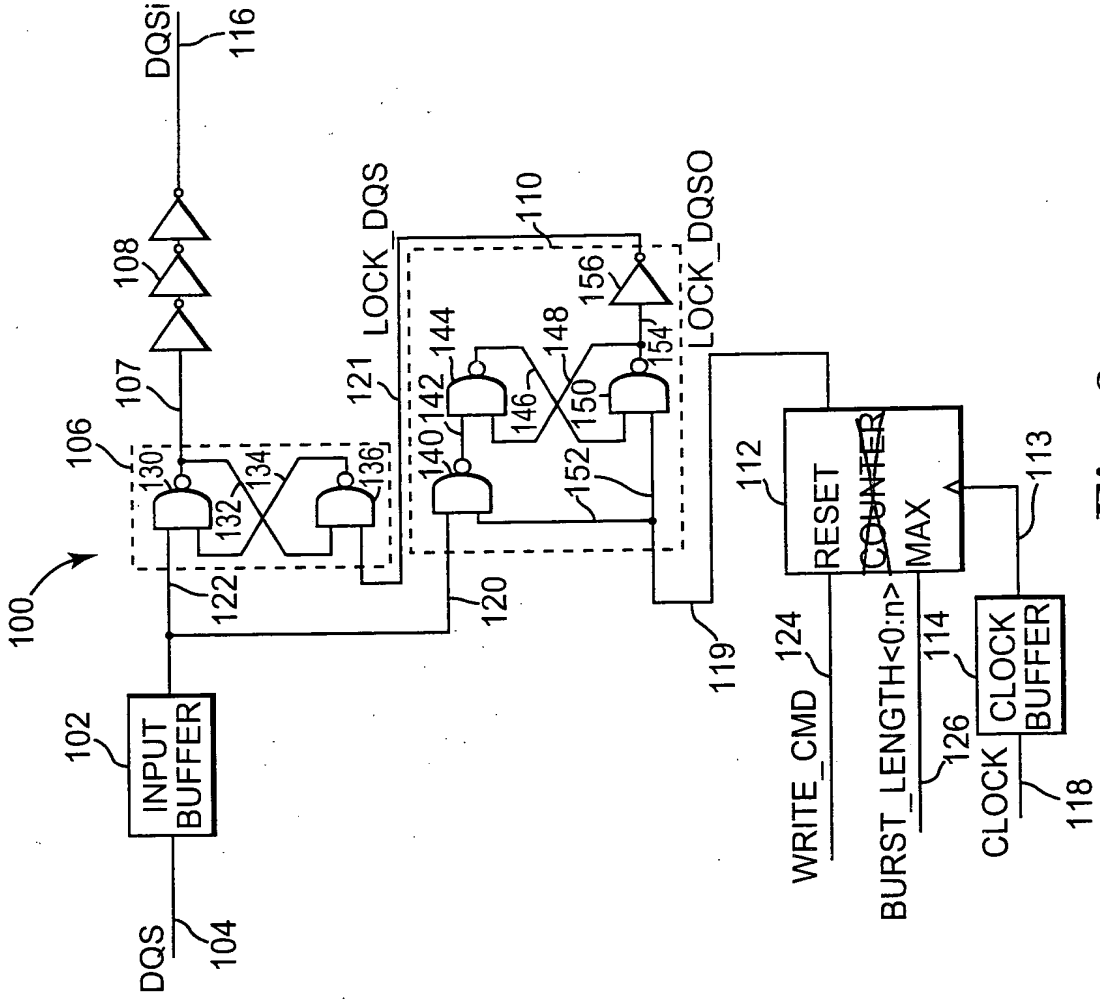

Fig. 3